Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-155. (Canceled)

156. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a stress-controlled dielectric membrane overlying the circuit devices.

157. (Previously Presented) The method of claim 156, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

158. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

159. (Previously Presented) The method of claim 158, wherein said stress is tensile.

160. (Previously Presented) The method of claim 157, comprising forming at least one of the at least one stress-

controlled dielectric layers by depositing one or more stress-controlled dielectric films.

161. (Previously Presented) The method of claim 160, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

162. (Previously Presented) The method of claim 156, wherein the stress-controlled dielectric membrane is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric membrane.

163. (Previously Presented) The method of claim 162, wherein said stress is tensile.

164. (Previously Presented) The method of claim 156, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

165. (Previously Presented) The method of claim 156, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

166. (Previously Presented) The method of claim 165, wherein the integrated circuit is able to be thinned to about 50

microns or less throughout a full extent thereof while retaining its structural integrity.

167. (Previously Presented) The method of claim 156, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

168. (Previously Presented) The method of claim 167, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

169. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a stress-controlled dielectric layer overlying the circuit devices.

170. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

171. (Previously Presented) The method of claim 170, wherein said stress is tensile.

172. (Previously Presented) The method of claim 169, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

173. (Previously Presented) The method of claim 172, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

174. (Previously Presented) The method of claim 169, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

175. (Previously Presented) The method of claim 169, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

176. (Previously Presented) The method of claim 175, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

177. (Previously Presented) The method of claim 169, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

178. (Previously Presented) The method of claim 177, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

179. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface; and

forming circuitry on the principal surface of the substrate with a stress-controlled dielectric layer.

180. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

181. (Previously Presented) The method of claim 180, wherein said stress is tensile.

182. (Previously Presented) The method of claim 179, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

183. (Previously Presented) The method of claim 182, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

184. (Previously Presented) The method of claim 179, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

185. (Previously Presented) The method of claim 179, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

186. (Previously Presented) The method of claim 185, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

187. (Previously Presented) The method of claim 179, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

188. (Previously Presented) The method of claim 187, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

189. (Previously Presented) A method of using an integrated circuit having a stress-controlled dielectric layer and interconnections formed passing through the stress-controlled dielectric layer, the method comprising:

transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

190. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

191. (Previously Presented) The method of claim 190, wherein said stress is tensile.

192. (Previously Presented) The method of claim 189, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

193. (Previously Presented) The method of claim 192, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

194. (Previously Presented) The method of claim 189, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

195. (Previously Presented) The method of claim 194, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

196. (Previously Presented) The method of claim 189, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

197. (Previously Presented) The method of claim 196, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

198. (Previously Presented) A method of using an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, interconnect circuitry interconnecting the data source and the data sink, the interconnect circuitry formed within a stress-controlled dielectric layer, the method comprising:

transferring a plurality of data bytes between the data source and data sink of the interconnect circuitry of the integrated circuit.

199. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

200. (Previously Presented) The method of claim 199, wherein said stress is tensile.

201. (Previously Presented) The method of claim 198, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

202. (Previously Presented) The method of claim 201, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

203. (Previously Presented) The method of claim 198, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

204. (Previously Presented) The method of claim 203, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

205. (Previously Presented) The method of claim 198, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

206. (Previously Presented) The method of claim 205, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

207. (Previously Presented) The method of claim 156, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

208. (Previously Presented) The method of claim 156, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

209. (Previously Presented) The method of claim 179, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

210. (Previously Presented) The method of claim 179, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

211. (Previously Presented) The method of claim 189, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

212. (Previously Presented) The method of claim 189, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

213. (Previously Presented) The method of claim 198, further comprising:

a second integrated circuit overlying the integrated circuit; and

interconnect connecting portions of the circuitry of the second integrated circuit and the integrated circuit.

214. (Previously Presented) The method of claim 198, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

215. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

216. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

217. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

218. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated

circuit is caused to have a thickness of about 50 microns or less.

219. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer are caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

220. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming a stress-controlled dielectric membrane overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

221. (Previously Presented) The method of claim 220, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

222. (Previously Presented) The method of claim 220, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

223. (Previously Presented) The method of claim 220, further comprising removing a major portion of the substrate.

224. (Previously Presented) The method of claim 223, wherein the major portion of the substrate is removed prior to forming said circuitry.

225. (Previously Presented) The method of claim 223, wherein the major portion of the substrate is removed after forming said circuitry.

226. (Previously Presented) The method of claim 220, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

227. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric membrane.

228. (Previously Presented) The method of claim 227, wherein said stress is tensile.

229. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

230. (Previously Presented) The method of claim 220, wherein the major portion of the substrate is removed prior to forming said circuitry.

231. (Previously Presented) The method of claim 220, wherein the major portion of the substrate is removed after forming said circuitry.

232. (Previously Presented) The method of claim 220, comprising forming the stress-controlled dielectric membrane by deposition of one or more stress-controlled dielectric films.

233. (Previously Presented) The method of claim 232, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

234. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming a stress-controlled dielectric layer overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

235. (Previously Presented) The method of claim 234, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

236. (Previously Presented) The method of claim 234, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

237. (Previously Presented) The method of claim 236, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

238. (Previously Presented) The method of claim 234, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

239. (Previously Presented) The method of claim 234, further comprising removing a major portion of the substrate.

240. (Previously Presented) The method of claim 239, wherein the major portion of the substrate is removed prior to forming said circuitry.

241. (Previously Presented) The method of claim 239, wherein the major portion of the substrate is removed after forming said circuitry.

242. (Previously Presented) The method of claim 234, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

243. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

244. (Previously Presented) The method of claim 243, wherein said stress is tensile.

245. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices;

forming a stress-controlled dielectric layer overlying said active devices; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

246. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed prior to forming said circuitry.

247. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed after forming said circuitry.

248. (Previously Presented) The method of claim 245, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

249. (Previously Presented) The method of claim 248, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

250. (Previously Presented) The method of claim 245, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

251. (Currently Amended) The method of claim [[245]] 156, wherein the major portion of the substrate is removed prior to forming said circuitry.

252. (Currently Amended) The method of claim [[245]] 156, wherein the major portion of the substrate is removed after forming said circuitry.

253. (Previously Presented) The method of claim 245, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

254. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

255. (Previously Presented) The method of claim 254, wherein said stress is tensile.

256. (Previously Presented) The method of claim 220, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

257. (Previously Presented) The method of claim 220, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

258. (Previously Presented) The method of claim 234, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

259. (Previously Presented) The method of claim 234, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

260. (Previously Presented) The method of claim 245, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

261. (Previously Presented) The method of claim 245, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

262. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

263. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have

a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

264. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

265. (Previously Presented) The method of claim 169, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

266. (Previously Presented) The method of claim 169, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

267. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture

strength of the at least one or more stress-controlled dielectric layers.

268. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible.

269. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to be elastic and the at least one or more stress-controlled dielectric layers are caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

270. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to be elastic and the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

271. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible.

272. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric

layers are caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

273. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be elastic and the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

274. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

275. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

276. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

277. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

278. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

279. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

280. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

281. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

282. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to

have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

283. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

284. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

285. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

286. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

287. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2

to 100 times less than the fracture strength of the stress-controlled dielectric layer.

288. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

289. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

290. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

291. (Previously Presented) The method of claim 245, wherein stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

292. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a low stress dielectric layer overlying the circuit devices.

293. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the low stress dielectric layer.

294. (Previously Presented) The method of claim 293, wherein said stress is tensile.

295. (Previously Presented) The method of claim 292, comprising forming the low stress dielectric layer by deposition of one or more low stress dielectric films.

296. (Previously Presented) The method of claim 295, comprising depositing at least one of the one or more of the low stress dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

297. (Previously Presented) The method of claim 292, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

298. (Previously Presented) The method of claim 292, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof.

299. (Previously Presented) The method of claim 292, further comprising removing a major portion of the substrate throughout a full extent thereof.

300. (Previously Presented) The method of claim 299, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

301. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

302. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is caused to be at least one of elastic and substantially flexible.

303. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to be at least one of elastic and substantially flexible.

304. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is caused to have a

stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less and the low stress dielectric layer is caused to be at least one of elastic and substantially flexible.

305. (Previously Presented) The method of claim 292, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

306. (Previously Presented) The method of claim 292, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

307. (Previously Presented) A method of fabricating circuitry comprising the steps of:

providing a substrate having a principal surface;

forming circuit devices on the principal surface;

forming a low stress dielectric layer overlying the circuit devices; and

forming interconnections ~~on~~ within the low stress dielectric layer between the circuit devices, wherein the

interconnections are at least one of electrical and optical interconnections.

308. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the low stress dielectric layer.

309. (Previously Presented) The method of claim 308, wherein said stress is tensile.

310. (Previously Presented) The method of claim 307, comprising forming the low stress dielectric layer by deposition of one or more low stress dielectric films.

311. (Previously Presented) The method of claim 310, comprising depositing at least one of the one or more of low stress dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

312. (Previously Presented) The method of claim 307, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

313. (Previously Presented) The method of claim 307, wherein the circuitry is able to be thinned to about 50 microns or less throughout a full extent thereof.

314. (Previously Presented) The method of claim 307, further comprising removing a major portion of the substrate throughout a full extent thereof.

315. (Previously Presented) The method of claim 314, wherein the circuitry is caused to have a thickness of about 50 microns or less.

316. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the circuitry is caused to have a thickness of about 50 microns or less.

317. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is caused to be at least one of elastic and substantially flexible.

318. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the low stress dielectric layer.

319. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is caused to be elastic and the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the circuitry is caused to have a thickness of about 50 microns or less.

320. (Previously Presented) The method of claim 307, further comprising:

providing a second circuitry overlying the circuitry; and

providing an interconnect that connects portions of the circuitry of the second circuitry and the circuitry.

321. (Previously Presented) The method of claim 307, further comprising:

providing a plurality of circuits overlying the circuitry; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of circuitry and the circuitry.

322. (Previously Presented) A method of fabricating interconnect circuitry comprising the steps of:

providing a substrate having a principal surface;

forming a low stress dielectric layer overlying the principal surface; and

forming interconnections within the low stress dielectric layer, wherein the interconnections are at least one of electrical and optical interconnections.

323. (Previously Presented) The method of claim 322, wherein the low stress dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the low stress dielectric layer.

324. (Previously Presented) The method of claim 323, wherein said stress is tensile.

325. (Previously Presented) The method of claim 322, comprising forming the low stress dielectric layer by deposition of one or more low stress dielectric films.

326. (Previously Presented) The method of claim 325, comprising depositing at least one of the one or more of low stress dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

327. (Previously Presented) The method of claim 322, wherein the low stress dielectric layer is caused to be at least one of elastic and substantially flexible.

328. (Previously Presented) The method of claim 322, wherein the low stress dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the low stress dielectric layer.

329. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming an elastic dielectric layer overlying the circuit devices.

330. (Previously Presented) The method of claim 329, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

331. (Previously Presented) The method of claim 330, wherein said stress is tensile.

332. (Previously Presented) The method of claim 329, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

333. (Previously Presented) The method of claim 332, comprising depositing at least one of the one or more of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

334. (Previously Presented) The method of claim 329, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

335. (Previously Presented) The method of claim 329, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

336. (Previously Presented) The method of claim 335, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

337. (Previously Presented) The method of claim 329, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

338. (Previously Presented) The method of claim 337, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

339. (Previously Presented) The method of claim 329, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

340. (Previously Presented) The method of claim 329, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

341. (Previously Presented) The method of claim 329, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

342. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming an elastic dielectric layer overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

343. (Previously Presented) The method of claim 342, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

344. (Previously Presented) The method of claim 343, wherein said stress is tensile.

345. (Previously Presented) The method of claim 342, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

346. (Previously Presented) The method of claim 342, comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

347. (Previously Presented) The method of claim 346, comprising depositing at least one of the one or more of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

348. (Previously Presented) The method of claim 342, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

349. (Previously Presented) The method of claim 342, further comprising removing a major portion of the substrate.

350. (Previously Presented) The method of claim 349, wherein the major portion of the substrate is removed prior to forming said circuitry.

351. (Previously Presented) The method of claim 349, wherein the major portion of the substrate is removed after forming said circuitry.

352. (Previously Presented) The method of claim 342, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

353. (Previously Presented) The method of claim 342, wherein the elastic dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

354. (Previously Presented) The method of claim 342, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

355. (Previously Presented) The method of claim 342, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

356. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices;

forming an elastic dielectric layer overlying said active devices; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

357. (Previously Presented) The method of claim 356, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

358. (Previously Presented) The method of claim 357, wherein said stress is tensile.

359. (Previously Presented) The method of claim 356, wherein the major portion of the substrate is removed prior to forming said circuitry.

360. (Previously Presented) The method of claim 356, wherein the major portion of the substrate is removed after forming said circuitry.

361. (Previously Presented) The method of claim 356, comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

362. (Previously Presented) The method of claim 361, comprising depositing at least one of the one or more of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

363. (Previously Presented) The method of claim 356, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

364. (Previously Presented) The method of claim 356, wherein the major portion of the substrate is removed prior to forming said circuitry.

365. (Previously Presented) The method of claim 356, wherein the major portion of the substrate is removed after forming said circuitry.

366. (Previously Presented) The method of claim 356, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

367. (Previously Presented) The method of claim 356, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

368. (Previously Presented) The method of claim 356, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

369. (Previously Presented) The method of claim 356, wherein the elastic dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

370. (Previously Presented) A method of using an integrated circuit having an elastic dielectric layer and interconnections formed within and passing through the elastic dielectric layer, the method comprising:

transferring information through the interconnections formed passing through the elastic dielectric layer, wherein the interconnections are at least one of electrical and optical interconnections.

371. (Previously Presented) The method of claim 370, wherein the elastic dielectric layer is caused to have a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

372. (Previously Presented) The method of claim 371, wherein said stress is tensile.

373. (Previously Presented) The method of claim 370, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

374. (Previously Presented) The method of claim 373, comprising depositing at least one of the one or more of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

375. (Previously Presented) The method of claim 370, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

376. (Previously Presented) The method of claim 375, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

377. (Previously Presented) The method of claim 370, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

378. (Previously Presented) The method of claim 377, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

379. (Previously Presented) The method of claim 370, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

380. (Previously Presented) The method of claim 370, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

381. (Previously Presented) The method of claim 370, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

382. (Previously Presented) A method of using an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, interconnect circuitry interconnecting the data source and the data sink, the interconnect circuitry formed within an elastic dielectric layer, the method comprising:

transferring a plurality of data bytes between the data source and data sink of the interconnect circuitry of the integrated circuit.

383. (Previously Presented) The method of claim 382, wherein the elastic dielectric layer is caused to have a stress

of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the elastic dielectric layer.

384. (Previously Presented) The method of claim 383, wherein said stress is tensile.

385. (Previously Presented) The method of claim 382, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

386. (Previously Presented) The method of claim 385, comprising depositing at least one of the one or more of the elastic dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

387. (Previously Presented) The method of claim 382, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

388. (Previously Presented) The method of claim 387, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

389. (Previously Presented) The method of claim 382, further comprising removing a major portion of the substrate

throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

390. (Previously Presented) The method of claim 389, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

391. (Previously Presented) The method of claim 382, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

392. (Previously Presented) The method of claim 382, further comprising:

a second integrated circuit overlying the integrated circuit; and

interconnect connecting portions of the circuitry of the second integrated circuit and the integrated circuit.

393. (Previously Presented) The method of claim 382, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

394. (Previously Presented) The method of claim 156, further comprising forming a barrier layer in the substrate

parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

395. (Previously Presented) The method of claim 169, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

396. (Previously Presented) The method of claim 179, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry, the principal surface overlying the barrier layer.

397. (Previously Presented) The method of claim 220, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

398. (Previously Presented) The method of claim 234, further comprising: providing a principal surface on the substrate; and
forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

399. (Previously Presented) The method of claim 245, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

400. (Previously Presented) The method of claim 292, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

401. (Previously Presented) The method of claim 307, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

402. (Previously Presented) The method of claim 329, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

403. (Previously Presented) The method of claim 342, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having

active devices, the principal surface overlying the barrier layer.

404. (Previously Presented) The method of claim 356, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

405. (Previously Presented) The method of claim 329, further comprising forming the elastic dielectric layer by deposition of one or more stress-controlled dielectric films.

406. (Previously Presented) The method of claim 405, wherein the stress-controlled dielectric films are caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric films.

407. (Previously Presented) The method of claim 406, wherein the stress is tensile.

408. (Previously Presented) The method of claim 405, further comprising depositing one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

409. (Previously Presented) The method of claim 157, wherein the stress-controlled dielectric layers are formed from at least one of an inorganic dielectric material and an organic dielectric material.

410. (Previously Presented) The method of claim 409, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

411. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

412. (Previously Presented) The method of claim 411, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

413. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

414. (Previously Presented) The method of claim 413, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

415. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is formed from at

least one of an inorganic dielectric material and an organic dielectric material.

416. (Previously Presented) The method of claim 415, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

417. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

418. (Previously Presented) The method of claim 417, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

419. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane is formed from at least one of an inorganic dielectric material and an organic dielectric material.

420. (Previously Presented) The method of claim 419, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

421. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

422. (Previously Presented) The method of claim 421, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

423. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

424. (Previously Presented) The method of claim 423, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

425. (Canceled)

426. (Canceled)

427. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

428. (Previously Presented) The method of claim 427, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

429. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

430. (Previously Presented) The method of claim 429, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

431. (Previously Presented) The method of claim 322, wherein the low stress dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

432. (Previously Presented) The method of claim 431, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

433. (Previously Presented) The method of claim 329, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

434. (Previously Presented) The method of claim 433, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

435. (Previously Presented) The method of claim 342, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

436. (Previously Presented) The method of claim 435, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

437. (Previously Presented) The method of claim 356, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

438. (Previously Presented) The method of claim 437, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

439. (Previously Presented) The method of claim 370, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

440. (Previously Presented) The method of claim 439, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

441. (Previously Presented) The method of claim 382, wherein the elastic dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

442. (Previously Presented) The method of claim 441, wherein the inorganic dielectric material is one of silicon dioxide and silicon nitride.

443. (Previously Presented) The method of claim 329, wherein the elastic dielectric layer is caused to be substantially flexible.

444. (Previously Presented) The method of claim 342, wherein the elastic dielectric layer is caused to be substantially flexible.

445. (Previously Presented) The method of claim 356, wherein the elastic dielectric layer is caused to be substantially flexible.

446. (Previously Presented) The method of claim 370, wherein the elastic dielectric layer is caused to be substantially flexible.

447. (Previously Presented) The method of claim 382, wherein the elastic dielectric layer is caused to be substantially flexible.

448. (Previously Presented) The method of claim 157, further comprising a plurality of interconnect conductors formed within at least one of the at least one or more stress-controlled dielectric layers, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

449. (Previously Presented) The method of claim 156, further comprising at least one flexible integrated circuit overlying the integrated circuit.

450. (Previously Presented) The method of claim 156, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

451. (Previously Presented) The method of claim 157, wherein at least one of the at least one or more stress-controlled dielectric layers is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

452. (Previously Presented) The method of claim 157, wherein at least one of the at least one or more stress-controlled dielectric layers is formed at a temperature of about 400°C.

453. (Previously Presented) The method of claim 169, further comprising a plurality of interconnect conductors formed within the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

454. (Previously Presented) The method of claim 169, further comprising at least one flexible integrated circuit overlying the integrated circuit.

455. (Previously Presented) The method of claim 169, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

456. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

457. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

458. (Previously Presented) The method of claim 179, further comprising a plurality of interconnect conductors formed within the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

459. (Previously Presented) The method of claim 179, further comprising at least one flexible integrated circuit overlying the integrated circuit.

460. (Previously Presented) The method of claim 179, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

461. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

462. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

463. (Previously Presented) The method of claim 189, further comprising at least one flexible integrated circuit overlying the integrated circuit.

464. (Previously Presented) The method of claim 189, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

465. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

466. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a withstand temperature of about 400°C or less.

467. (Previously Presented) The method of claim 198, further comprising at least one flexible integrated circuit overlying the integrated circuit.

468. (Previously Presented) The method of claim 198, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

469. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

470. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

471. (Previously Presented) The method of claim 229, further comprising a plurality of interconnect conductors formed within at least one of the at least one or more stress-controlled dielectric layers, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

472. (Previously Presented) The method of claim 220, further comprising at least one flexible integrated circuit overlying the integrated circuit.

473. (Previously Presented) The method of claim 220, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

474. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

475. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are formed at a temperature of about 400°C.

476. (Previously Presented) The method of claim 234, further comprising a plurality of interconnect conductors formed within the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

477. (Previously Presented) The method of claim 234, further comprising at least one flexible integrated circuit overlying the integrated circuit.

478. (Previously Presented) The method of claim 234, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

479. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

480. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

481. (Previously Presented) The method of claim 245, further comprising a plurality of interconnect conductors formed within the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

482. (Previously Presented) The method of claim 245, further comprising at least one flexible integrated circuit overlying the integrated circuit.

483. (Previously Presented) The method of claim 245, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

484. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

485. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

486. (Previously Presented) The method of claim 292, further comprising a plurality of interconnect conductors formed

within the low stress dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

487. (Previously Presented) The method of claim 292, further comprising at least one flexible integrated circuit overlying the integrated circuit.

488. (Previously Presented) The method of claim 292, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

489. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

490. (Previously Presented) The method of claim 292, wherein the low stress dielectric layer is formed at a temperature of about 400°C.

491. (Previously Presented) The method of claim 307, further comprising at least one flexible integrated circuit overlying the integrated circuit.

492. (Previously Presented) The method of claim 307, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

493. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

494. (Previously Presented) The method of claim 307, wherein the low stress dielectric layer is formed at a temperature of about 400°C.

495. (Previously Presented) The method of claim 322, further comprising at least one flexible integrated circuit overlying the interconnect circuitry.

496. (Previously Presented) The method of claim 322, wherein the interconnect circuitry is capable of forming at least one of a substantially flexible interconnect circuitry and an elastic interconnect circuitry.

497. (Previously Presented) The method of claim 322, wherein the low stress dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

498. (Previously Presented) The method of claim 322, wherein the low stress dielectric layer is formed at a temperature of about 400°C.

499. (Previously Presented) The method of claim 329, further comprising a plurality of interconnect conductors formed

within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

500. (Previously Presented) The method of claim 329, further comprising at least one flexible integrated circuit overlying the integrated circuit.

501. (Previously Presented) The method of claim 329, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

502. (Previously Presented) The method of claim 329, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

503. (Previously Presented) The method of claim 329, wherein the elastic dielectric layer is formed at a temperature of about 400°C.

504. (Previously Presented) The method of claim 342, further comprising a plurality of interconnect conductors formed within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

505. (Previously Presented) The method of claim 342, further comprising at least one flexible integrated circuit overlying the integrated circuit.

506. (Previously Presented) The method of claim 342, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

507. (Previously Presented) The method of claim 342, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

508. (Previously Presented) The method of claim 342, wherein the elastic dielectric layer is formed at a temperature of about 400°C.

509. (Previously Presented) The method of claim 356, further comprising a plurality of interconnect conductors formed within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

510. (Previously Presented) The method of claim 356, further comprising at least one flexible integrated circuit overlying the integrated circuit.

511. (Previously Presented) The method of claim 356, wherein the integrated circuit is capable of forming at least

one of a substantially flexible integrated circuit and an elastic integrated circuit.

512. (Previously Presented) The method of claim 356, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

513. (Previously Presented) The method of claim 356, wherein the elastic dielectric layer is formed at a temperature of about 400°C.

514. (Previously Presented) The method of claim 370, further comprising at least one flexible integrated circuit overlying the integrated circuit.

515. (Previously Presented) The method of claim 370, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

516. (Previously Presented) The method of claim 370, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

517. (Previously Presented) The method of claim 370, wherein the elastic dielectric layer is caused to have a withstand temperature of about 400°C or less.

518. (Previously Presented) The method of claim 382, further comprising a plurality of interconnect conductors formed within the elastic dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

519. (Previously Presented) The method of claim 382, further comprising at least one flexible integrated circuit overlying the integrated circuit.

520. (Previously Presented) The method of claim 382, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

521. (Previously Presented) The method of claim 382, wherein the elastic dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

522. (Previously Presented) The method of claim 382, wherein the elastic dielectric layer is caused to have a withstand temperature of about 400°C or less.